1 Graphical symbols for binary logic elements

IEC 60617 DB contains graphical symbols that have been developed to represent logic functions. They are intended also to represent physical devices or combinations of physical devices capable of carrying out these functions. The symbols have been prepared with a view to electrical applications, but many can also be applied to non-electrical devices, for example pneumatic, hydraulic or mechanical.

2 General notes

2.1 For explanation of "logic states", "logic levels", etc., see 7.1.4.1.1 of IEC 61082-1.

2.2 The symbols 0 and 1 are used to identify the two logic states of a binary variable. These states are referred to as 0-state and 1 -state.

2.3 A binary variable may be equated to any physical quantity for which two distinct ranges can be defined. These distinct ranges are referred to as logic levels and are denoted H and L. H is used to denote the logic level with the more positive algebraic value, and L is used to denote the logic level with the less positive algebraic value.

2.4 In the case of a system in which logic states are equated with other qualities of a physical quantity (for example positive or negative pulses, presence or absence of a pulse), H and L may be used to represent these qualities or may be replaced by more suitable designations.

3 Explanation of terms

To facilitate understanding of the descriptions for the binary logic elements, it is useful to define three terms.

3.1 "Internal logic state" describes a logic state assumed to exist inside a symbol outline at an input or an output.

3.2 "External logic state" describes a logic state assumed to exist outside a symbol outline:
- on an input line prior to any external qualifying symbol at that input, or
- on an output line beyond any external qualifying symbol at that output.

3.3 "Logic level" describes the physical quality assumed to represent a logic state of a binary variable (see clauses 2.2 and 2.3).

For illustrations, see A00269_Illustration_a_EN.pdf below.

4 Composition of the symbol - Symbol construction

4.1 A symbol comprises an outline or combination of outlines together with one or more qualifying symbols.

Application of the symbols requires in addition the representation of input and output lines.

For illustrations, see A00269_Illustration_b_EN.pdf below.

The single asterisks (*) denote possible positions for qualifying symbols relating to inputs and outputs.

If and only if the function of an element is completely determined by the qualifying symbols associated with its inputs and/or outputs, no general qualifying symbol is needed.

4.2 General additional information may be included in a symbol outline as described in IEC 61082-1.

4.3 Information not standardized in this standard relating to a specific input [output] may be shown in square brackets inside the outline adjacent to the relevant input [output] and should follow [precede] any qualifying symbols applying to the input [output] as shown in symbol S01592 (12-28-14).

Additional information relating to the general logic function of the element may be shown in

square brackets inside the outline.

4.4 All outputs of an element represented by a single un-subdivided symbol always have identical internal logic states determined by the function of the element except when indicated otherwise by an associated qualifying symbol or label inside the symbol outline. The subdivision of a symbol and the qualifying symbols referred to here include those explicitly shown and those only implied according to the simplification rules of clause 6.3.

4.5 In some figures, lowercase letters which are not part of the symbols have been shown outside the outline just to identify the inputs [outputs] as referred to in the description.

4.6 The symbols and descriptions in this standard are intended for signal flow from left to right. If a symbol is instead intended for right-to-left flow, this is explicitly stated in the description of the symbol or indicated in the symbol itself.

When interpreting a symbol, one should assume, unless otherwise indicated, that a terminal shown on the left with respect to the normal reading orientation of the labels inside the symbol is an input, and that one shown on the right is an output. Inputs may also be shown on the right and outputs on the left if it aids the layout of the diagram or better conveys the structure of the device.

The direction of signal flow shall be clearly implied or indicated. Explicit indication may be done by using qualifying symbols that inherently indicate the direction of signal flow (such as qualifying symbols defined only for inputs or only for outputs, or general qualifying symbols that indicate flow direction) or by other symbols on the diagram that are connected to the terminal.

If the direction of signal flow on a terminal line is not otherwise obvious, that line shall be marked with an arrowhead (symbol S00099 (02-05-01)) pointing in the direction of signal flow or with the symbol for bidirectional signal flow (symbol S01547 (12-10-02)), whichever applies. No arrowhead shall touch the outline or any other qualifying symbol. See, for example, symbol S01599 (12-29-06).